





UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/469,497	12/22/1999	YUICHI KUNORI	49657-5	5036	
20277 75	90 11/20/2002				
MCDERMOTT WILL & EMERY			EXAMINER		
	600 13TH STREET, N.W. WASHINGTON, DC 20005-3096			SONG, JASMINE	
			ART UNIT	PAPER NUMBER	
			2188		
				DATE MAIL ED. 11/20/2002	

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No. 09/469,497 Examiner Jasmine Song The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.138(s). In no event, however, may a reply be timely filled after SIX (6) MONTTHS from the mailing date of this communication. - If the period for reply specified above its emission maintain the statutory minimum of thirty (20) days will be considered timely. - If NO period for reply specified above the maintenance statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above the maintenance statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above, the maintenance statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication, even if timely filled, may reduce any seared petient term adjustment. See 37 CFR 1.704(b). Status 1)			-	P				
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Jasmine Song Jass		09/469,497	KUNORI, YUICHI					
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Priority under 35 U.S.C. §§ 119 and 120								
	<u> </u>		,					
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).								
a)⊠ All b)□ Some * c)□ None of:								
1. Certified copies of the priority documents have been received.								
2. Certified copies of the priority documents have been received in Application No								
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 								
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).								
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.								
Attachment(s)								
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) Notice o						

U.S. Patent and Trademark Office PTO-326 (Rev. 04-01) Art Unit: 2188

Detailed Action

1. This Office Action is in responses to the amendment B filed on 08/30/2002, claims 1-23 are pending in the application, the claims 1-12 have been allowed, the claims 13-23 are represented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

3. The rejection of claim 16 under 35 USC § 112, second has been **withdrawn** due to amendment.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

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The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 13-14 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Egawa., U.S. Patent 6289,481 B1.

Regarding claim 13, Eagwa teaches that a method for reading a plurality of data from a non-volatile semiconductor memory device, said non-volatile semiconductor memory device including a memory cell (Fig.1 or Fig.6, element 5) storing said plurality of data and a data output node (Fig.1 or 6, element 8, output circuit is composed of output circuits 81 and 82 as shown in the Fig.6, col.5, lines 7-8) for outputting said data said method comprising the steps of:

reading a part of said plurality of data (Fig.6, lower digit data) from said memory cell (Fig.6, element 5 and col.6, lines 32-34);

outputting said part of said plurality of data (Fig.6, lower digit data) to said data output node (Fig.6 and col.6, lines 34-37);

reading another part of said plurality of data (Fig.6, higher digit data) from said memory cell (Fig.6, element 5 and col.6, lines 37-41); and

outputting said another part of said plurality of data (Fig.6, higher digit data) to said data output node (Fig.6 and col.6, lines 40-44).

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Regarding claim 14, Eagwa teaches that said step of outputting said part of said plurality of data overlaps with said step of reading another part of said plurality of data is taught as output lower digit data at time t3 and read the higher digit data at time t5, they overlap after t5 as shown in the Fig.9 (col.6, lines 33-41).

Regarding claim 18, Eagwa teaches that wherein said step of reading said another part of said plurality of data is performed after said step of reading said part of said plurality of data (Fig.9, col.6, lines 32-41).

Regarding claim 19, Eagwa teachers that wherein said step of outputting said another part of said plurality of data is performed after said step of outputting said part of said plurality of data (Fig.9, col.6, lines 32-41).

Claim Rejections - 35 USC § 103

- 6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claims 15,20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka., U.S. patent 6154393, in view of Egawa., U.S. Patent 6289,481 B1.

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Regarding claim 15, Otsuka teaches that a method for reading data from a non-volatile semiconductor memory device (Fig.5), said non-volatile semiconductor memory device including

a word line (Fig.5, col.8, lines 17-18),

first and second bit lines (Fig.5, col.8, lines 18-19),

a first memory cell coupled to said word line and said first bit line (Fig.5, col.8, lines 21-27),

a second memory cell coupled to said word line and said second bit line (Fig.5, col.8, lines 29-32), and

a data output node (Fig.5, element 28) for outputting said data from said first and second memory cells, said method comprising the steps of:

reading first data from said first memory cell with selectively activating said word line (Fig.5, col.8, lines 19-27);

outputting said first data to said data output node (Fig.5, col.8, lines 27-28);

reading second data from said second memory cell with selectively activating said word line (Fig.5, col.8, lines 29-32);

outputting said second data to said data output node (Fig.5, col.8, lines 32-33).

Otsuka does not specifically teach that the first and second memory cells are coupled to the same word line, therefore, Otsuka does not teach that the step of outputting data overlaps the step of reading data.

However, Egawa teaches that read the lower and higher digit data from the same memory cell (Fig.5) which means they are read from the same word line, he also

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teaches that the step of outputting data overlap the step of reading data which is taught as output lower digit data at time t3 and read the higher digit data at time t5, they overlap after t5 as shown in the Fig.9 (col.6, lines 33-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same word line for reading the first and second data and provide that the step of outputting data overlaps the step of reading data in the Otsuka's semiconductor memory device because this pipeline or parallel method would reduce the memory access time and speed up the data transfer, therefore, the whole system is enhanced and more efficient.

Regarding claim 20, Otsuka teaches that wherein said step of reading said second data is performed after said step of reading said first data (col.8, lines 24-32).

Regarding claim 21, Otsuka teaches that wherein said step of outputting said second data is performed after said step of outputting said first data (Fig.9).

8. Claims 16-17 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., U.S. Patent 5890192, in view of Toda et al., U.S. Patent 5708618.

Regarding claims 16 and 17, Lee teaches that a method for writing data to a non-volatile semiconductor memory device (Fig.3, element 4000), said non-volatile semiconductor memory device including a memory cell (Fig.3, element 400) storing first

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and second data (Fig.2, col.3, lines 46-52), said first and second registers (col.4, lines 46-52), said method comprising the steps of:

storing in said first register said first data input from the outside of said non-volatile semiconductor memory device (col.4,lines 56-60); writing said first data stored in said first register to said memory cell (col.4, lines 46-55); storing in said second register said second data input from the outside of said nonvolatile semiconductor memory device (col.4,lines 56-60); and writing said second data stored in said second register to said memory cell (col.4, lines 46-55).

Lee does not specifically teach that data from the first register and second register are written to the same memory cell, therefore, Lee fails to teach that the step of writing the first data overlaps with the step of storing the second data.

However, Toda teaches that data from the first register and second register are written to the same memory cell (col.2, lines 35-42) and the step of writing the first data overlaps with the step of storing the second data is taught as the write in and read out are proceeding simultaneously but actually they are carried out independently and asynchronously (Fig.4, col.6, lines 36 to col.7, lines 53).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same word line for reading the first and second data and provide that the step of outputting data overlaps the step of reading data in the Lee's EEPROM system because this pipeline or parallel method would reduce the memory access time and speed up the data transfer, therefore, the whole system is enhanced and more efficient.

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Regarding claim 22, Lee teaches that wherein said step of storing said second data is performed after said step of storing said first data is taught as latching the first and second data into the data register 404 and 405 sequentially (col.4, lines 50-52).

Regarding claim 23, Lee teaches that wherein said step of writing said second data is performed after said step of writing said first data (col.1, lines 37-40 and col.4, lines 46-49).

Response to Arguments

- 9. Applicant's arguments with respect to claims 13-17 have been considered but are moot in view of the new ground(s) of rejection.
- 10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).
- 11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

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12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do H Yoo can be reached on 703-308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

November 15, 2002

Reginald D. Bragdon REGINALD G. BRAGDON PRIMARY EXAMINER

IMPORTANT NOTICE

The Examiner's art unit number has changed from 2187 to 2188 due to the recent realignment of workgroup 2180. Please use art unit 2188 on all correspondence related to this case.
